With the exception of the enable prec
the WD1773 is identical to the WD17
is fully software compatible with the
WD1770-00 and WD1773-00 are comp
FD179X stepping rates, while the WD
stepping rates of 2, 3, 6, and 12 ms

The WD177X-00 devices all contain a
data separator which virtually elimina
components and adjustments associ

20	MO	MO (WD WD
21	WG	WR
22	WD	WR
23	$\overline{TR00}$	$\overline{TR}$
24	$\overline{IP}$	$\overline{IN}$
25	$\overline{WPRT}$	$\overline{WP}$

ARCHITECTURE

The primary sections of the Floppy
the Parallel Processor Interface a
Interface.

Data Shift Register – This 8-bit
serial data from the Read Data
Read operations and transfers ser
Data output during Write operat

Data Register – This 8-bit register
register during Disk Read and W
disk Read operations, the asse
transferred in parallel to the Dat
Data Shift Register. In Disk Writ
mation is transferred in paral
Register to the Data Shift Regis

When executing the Seek Co
Register holds the address of the

Timing and Control - All computer interface controls are generated t The internal device timing is genera nal crystal clock. The WD177X-00 modes of operation according DDEN.

When $\overline{\text{DDEN}}$ = 0, double density
When DDEN = 1, single density

AM Detector - The address mark de data and index address marks dur operations.

Data Separator - A digital data sep of a ring shift register and data logic provides read data and a rec AM detector.

ding to the state DDEN. When
density is selected. In either cas
at 8 MHz.

GENERAL DISK READ OPERATIO

Sector lengths of 128, 256, 512 or
in either FM or MFM formats
is placed to logical 1. For MFM
placed to a logical 0. Sector leng
at format time by the fourth byt

SECTOR LENGTH T	
SECTOR LENGTH FIELD (HEX)	NUM IN SE
00	
01	
02	
03	

m = Multiple Sector Flag (Bit 4)

m = 0, Single Sector
m = 1, Multiple Sector

H = Motor on Flag (Bit 3) (1770/

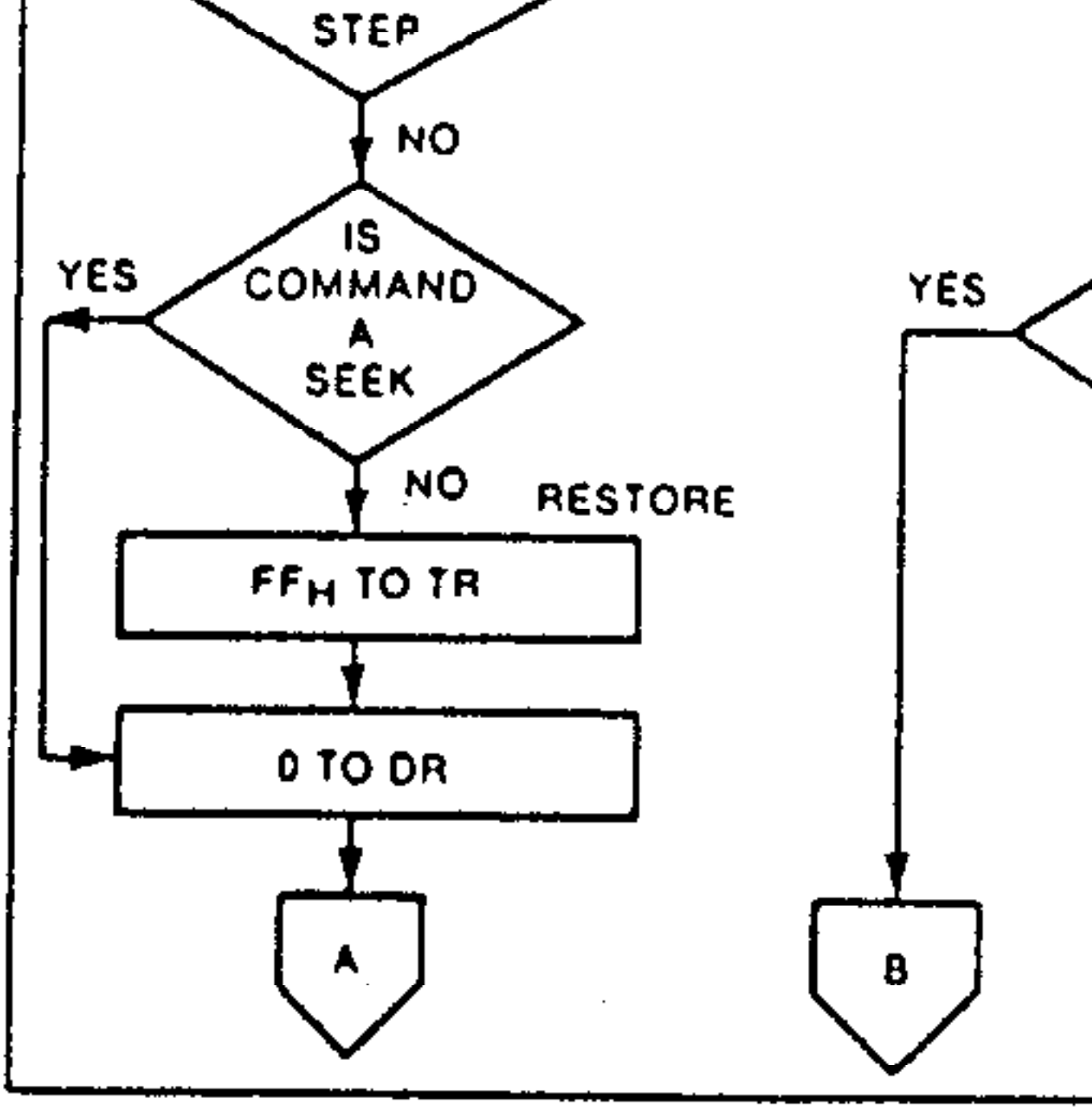
H = 0, Enable Spin-up Sequenc
H = 1, Disable Spin-up Sequen

S = Side Compare Flag (Bit 3) (

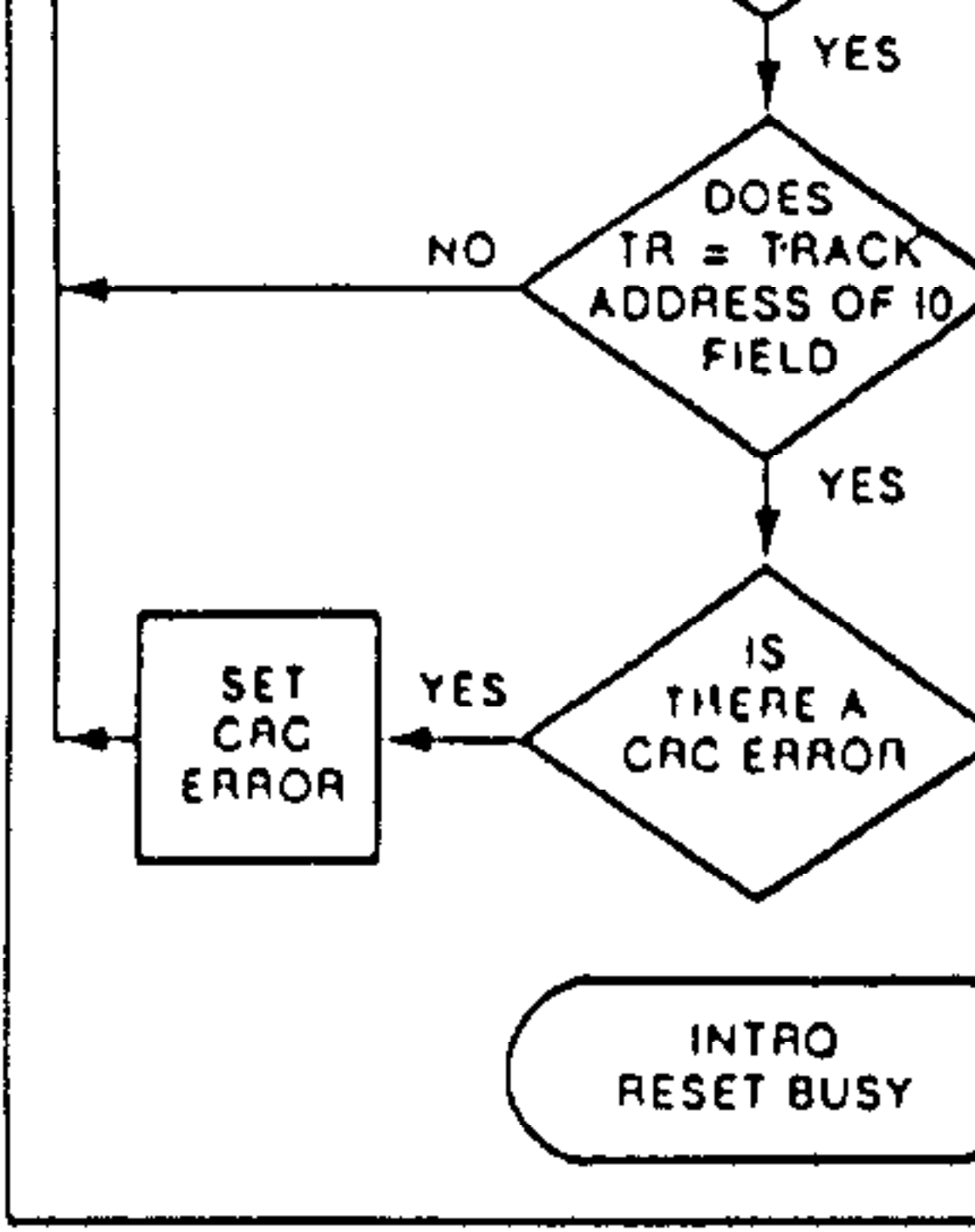
S = 0, Compare for side 0
S = 1, Compare ;for side 1
For all Type III commands bit 3

a_0 = Data Address Mark (Bit 0) (

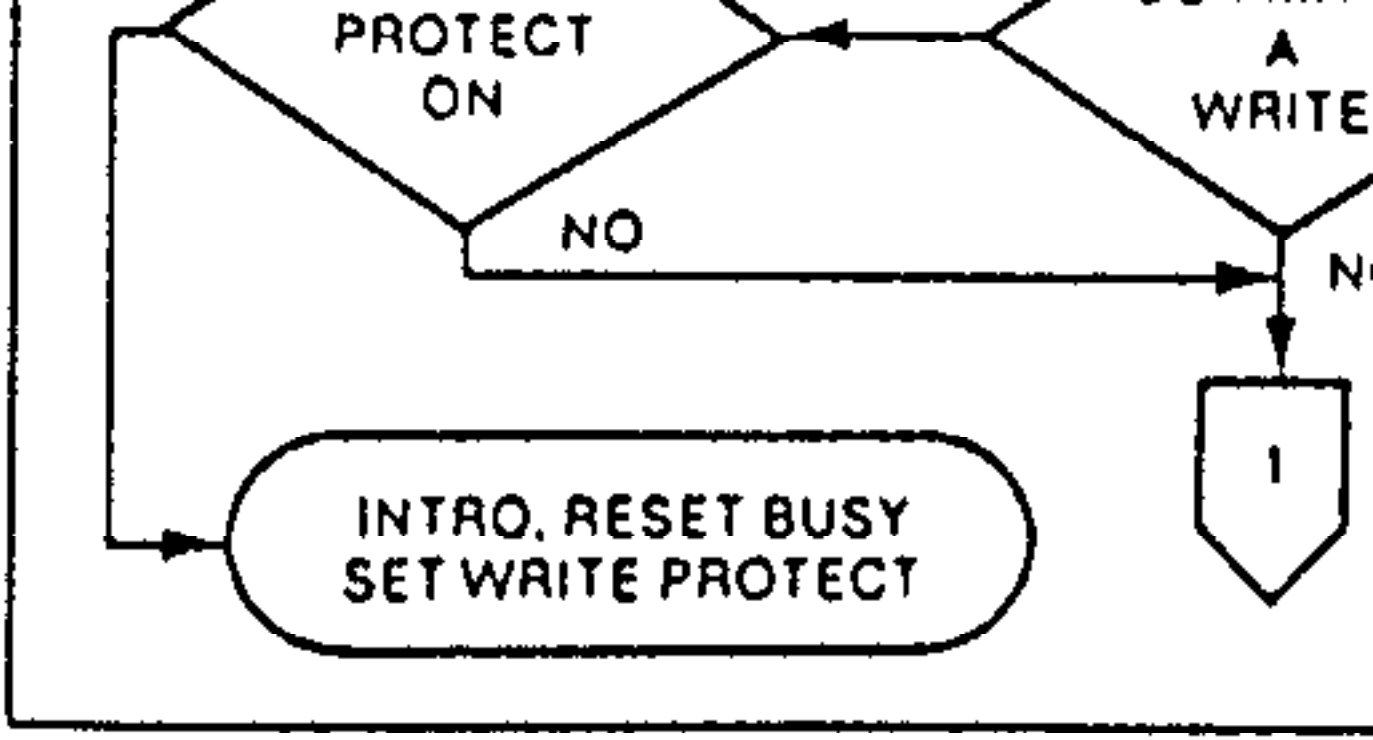
a_0 = 0, Write Normal Data Mark
a_0 = 1, Write Deleted Data Mar



TYPE I COMMAND FLOW



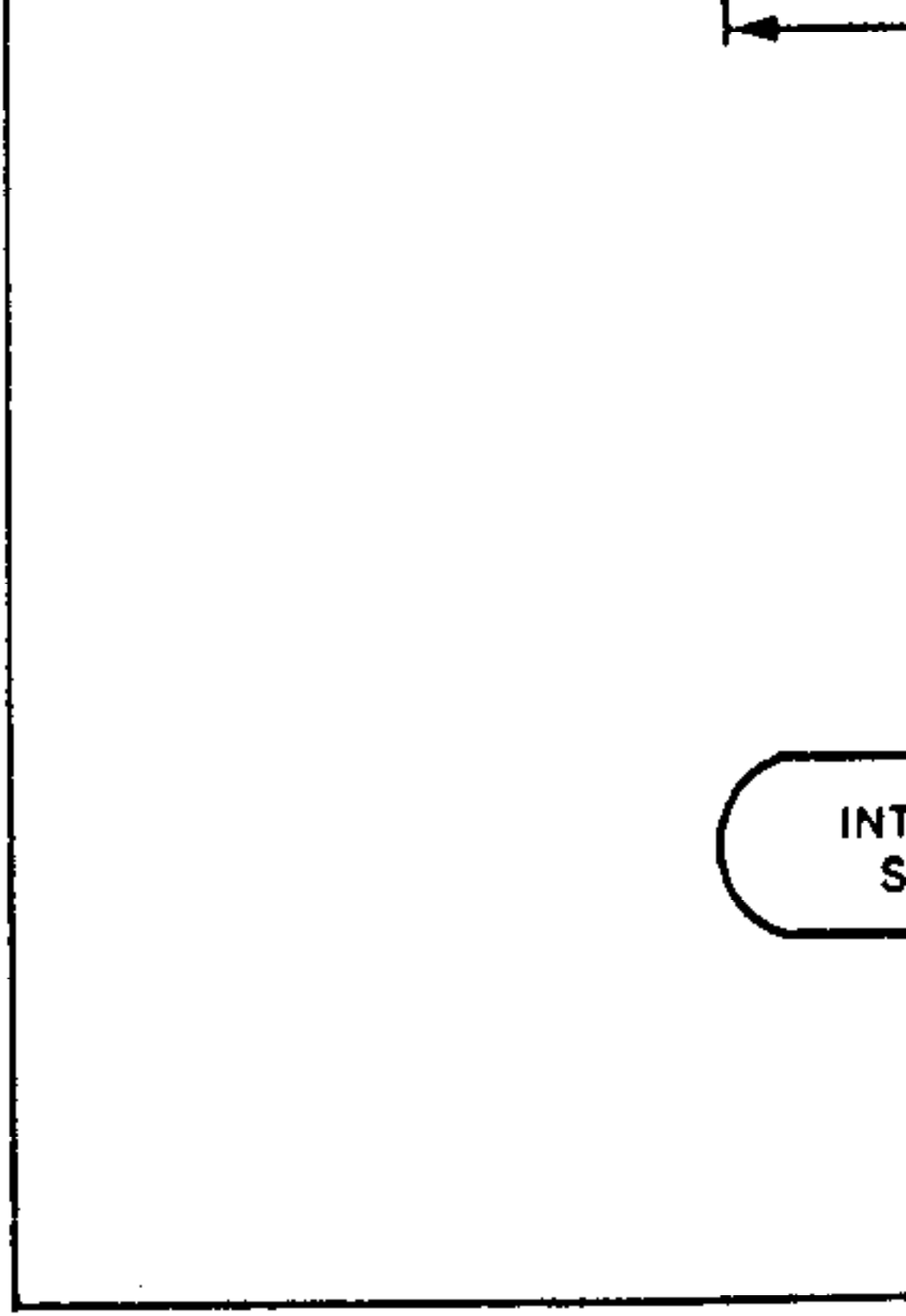
TYPE I COMMAND F

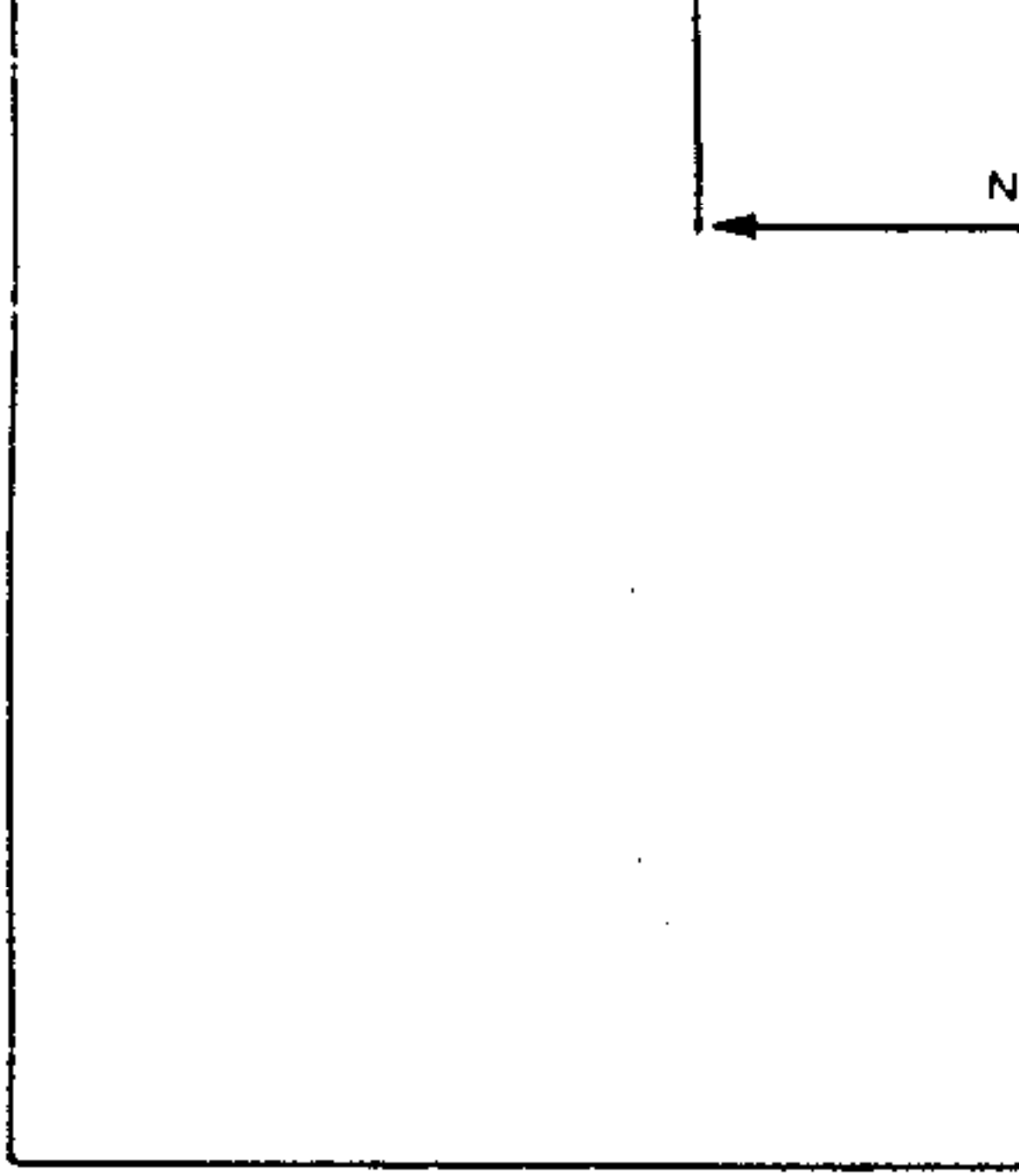


TYPE II COMMAND

tor Number of the ID field is compa
Sector Register. If there is no Sector ma
encountered ID field is read off the di
parisons again made. If the ID field CR
the data field is located and is either w
read from, depending upon the co
WD177X-00 finds an ID field with a Track
tor number, and CRC within four revol
disk, or, the Record Not Found Status bit
Bit 4) and the command is terminated wi

output is made active if the DRQ
DR is loaded by the computer). If
the command is terminated and
Bit is set. If the DRQ is servic
active and six bytes of zeroes i
12 bytes in double density are wr
Data Address Mark is then writt
termined by the a_0 field of the

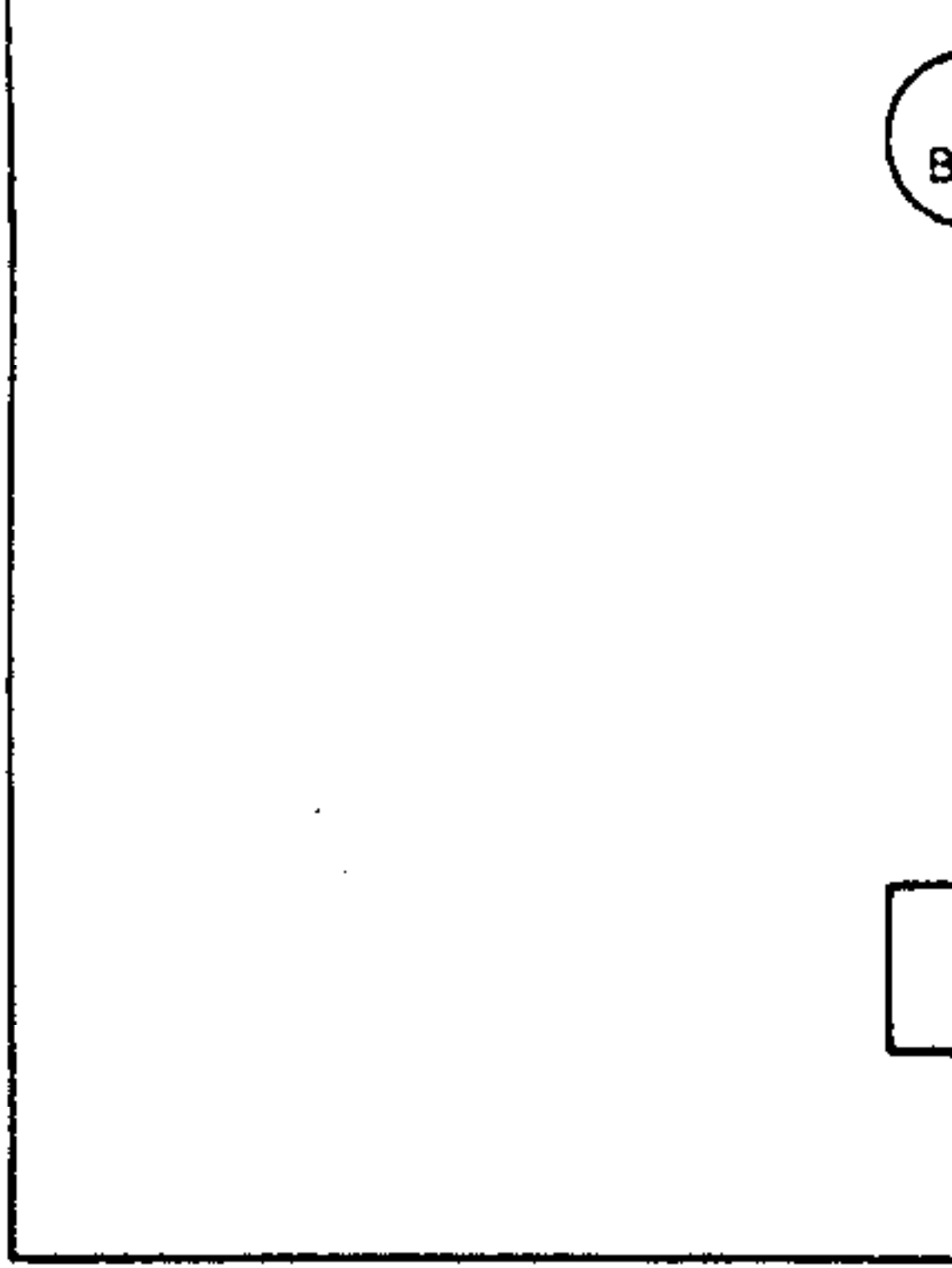

INT
S

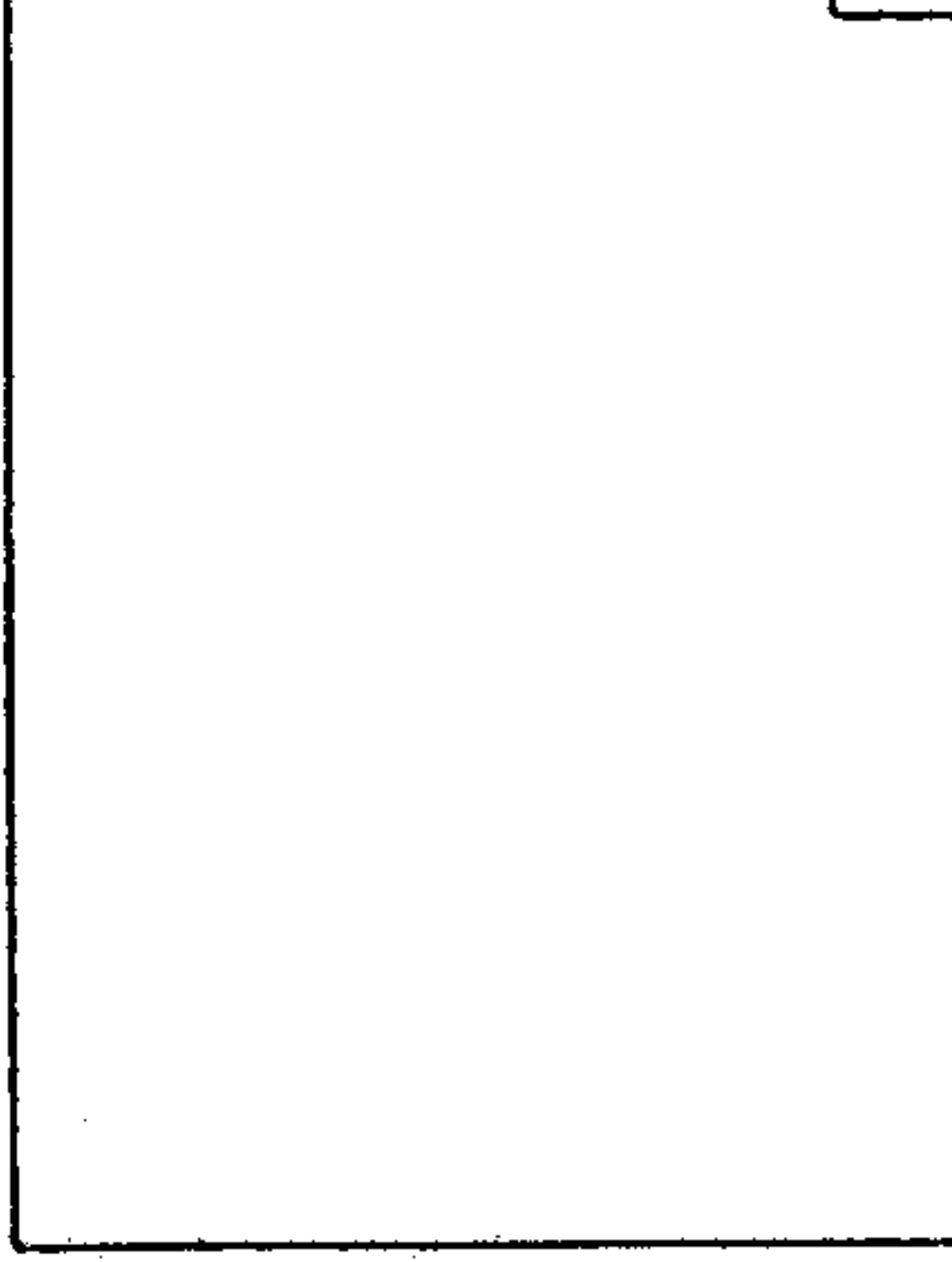

N

make it suitable for diagnostic p
no CRC checking is performed;

DATA PATTERN IN DR (HEX)	IN FM (DD
00 thru F4	Write 00
F5	Not Allow
F6	Not Allow
F7	Generate
F8 thru FB	Write F8
FC	Write FC
FD	Write FD
FE	Write FE,
FF	Write FF

*Missing clock transition betwe
**Missing clock transition betwe


8



Status Register

Upon receipt of any command, ex
rupt Command, the Busy Status B
of the status bits are updated or
command. If the Force Interrupt C
when there is a current comman
the Busy Status Bit is reset, and t
bits are unchanged. If the Force
is received when there is not a
under execution, the Busy Status
rest of the status bits are update
case, Status reflects the Type I

The user has the option of reading
through program control or using
DMA or interrupt methods. Whe
is read the DRQ bit in the Statu
DRQ line are automatically reset
Register also causes both DRQ

INDEX
PULSE
40 BYTES
'FF'
6 BYTES
'00'
ID
'FE'
TRACK
#

S4 RECORD NOT FOUND (RNF)	When s bit is re
S3 CRC ERROR	If S4 is error da
S2 LOST DATA/ BYTE	When s This bit status c
S1 DATA REQUEST INDEX	This bit Read O when u signal.
S0 BUSY	When s executi

S6 WRITE PROTECT	On Read Write Pr
S5 RECORD TYPE	On Read 1 = Del
S4 RECORD NOT FOUND (RNF)	When se is reset
S3 CRC ERROR	If S4 is s in data f
S2 LOST DATA	When se bit is res
S1 DATA REQUEST	This bit i Operatio updated.
S0 BUSY	When se

DRQ

READ ENABLE TIMING - $\overline{RE}$ suc

SYMBOL	CHARACT
t_{RE}	$\overline{RE}$ Pulse Width
t_{DRR}	DRQ Reset from
t_{DV}	Data Valid from
t_{DOH}	Data Hold from
	INTRQ Reset fr

Note: DRQ and INTRQ reset ar
(leading) of $\overline{WE}$. Worst ca

t_{WE}	WE Pulse Width
t_{DRW}	DRQ Reset from
t_{DS}	Data Setup to W
t_{DH}	Data Hold from
	INTRQ Reset fro

READ DATA TIMING:

CHARACTERISTIC
$\overline{\text{Raw Read}}$ Pulse Width
$\overline{\text{Raw Read}}$ Cycle Time

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERI
t_{CD1}	Clock Duty (low)
t_{CD2}	CLock Duty (high)
t_{STP}	Step Pulse Output
t_{DIR}	Dir Setup to Step
t_{MR}	Master Reset Pulse
t_{IP}	Index Pulse Width